EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	testing IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L2	0	IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L3	1	integrated circuit signal quality	USPAT	ADJ	OFF	2006/02/18 20:28
L4	13	"614040"	USPAT	OR	OFF	2006/02/18 20:34
L5	0	("signaltestingofintegratedcircuitchips").PN.	USPAT; USOCR	OR	OFF	2006/02/18 20:35
L6	0	signal testing of integrated circuit chips	USPAT	WITH	OFF	2006/02/18 20:36
L7	1187	power and ground bounce	USPAT	WITH	OFF	2006/02/18 21:27
L8	1	"614040"	US-PGPUB	OR	OFF	2006/02/18 21:26
L9	54	(power and ground bounce).ab.	USPAT	WITH	OFF	2006/02/18 21:27
L10	29089	(power and ground bounce).clm.	USPAT	OR	ON	2006/02/18 21:28
L11	14962	(power with ground bounce).clm.	USPAT	OR	ON	2006/02/18 21:28
L12	27	l9 and l11	USPAT	OR	OFF	2006/02/18 21:28

Patent Assignment Abstract of Title

Total Assignments: 1

Application #: 10614040 **Filing Dt:** 07/08/2003 **Patent #:** NONE **Issue Dt:**

PCT #: NONE **Publication #:** US20040123205 **Pub Dt:** 06/24/2004

Inventors: I-Ming Lin, Jen-Nan Liu

Title: Signal testing of integrated circuit chips

Assignment: 1

Reel/Frame: 014283 / 0911 **Received:** 07/22/2003 **Recorded:** 07/08/2003 **Mailed:** 01/28/2004 **Pages:** 2

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: LIN, I-MING **Exec Dt:** 03/26/2003

LIU, JEN NAN **Exec Dt:** 03/26/2003

Assignee: VIA TECHNOLOGIES, INC.
8F, 533, CHUNG-CHENG RD.
HSIN-TIEN
TAIPEI, TAIWAN R.O.C.

Correspondent: RABIN & BERDO, P.C.
STEVEN M. RABIN
1101 14TH STREET, N.W., SUITE 500
WASHINGTON, DC 20005

Search Results as of: 2/18/2006 9:14:10 P.M.

If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 571-272-3350
Web interface last modified: September 28, 2005

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	testing IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L2	0	IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L3	1	integrated circuit signal quality	USPAT	ADJ	OFF	2006/02/18 20:28
L4	13	"614040"	USPAT	OR	OFF	2006/02/18 20:34
L5	0	("signaltestingofintegratedcircuitchips").PN.	USPAT; USOCR	OR	OFF	2006/02/18 20:35
L6	0	signal testing of integrated circuit chips	USPAT	WITH	OFF	2006/02/18 20:36
L7	1187	power and ground bounce	USPAT	WITH	OFF	2006/02/18 21:06
L8	1	"614040"	US-PGPUB	OR	OFF	2006/02/18 21:06

Majority of search East cost Power Dd

PALM INTRANET

Day : Saturday
Date: 2/18/2006

Time: 21:09:54

Inventor Name Search Result

Your Search was:

Last Name = LIN
First Name = I-MING

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10055567	6877103	150	01/22/2002	BUS INTERFACE TIMING ADJUSTMENT DEVICE, METHOD AND APPLICATION CHIP	LIN, I-MING
10140994	6859150	150	05/09/2002	APPARATUS FOR READING KEYBOARD-COMMANDS OF A PORTABLE COMPUTER	LIN, I-MING
10194314	Not Issued	95	07/15/2002	SIGNAL COMPENSATION CIRCUIT OF A BUS	LIN, I-MING
10249439	Not Issued	94	04/10/2003	METHOD AND APPARATUS FOR USING A DYNAMIC RANDOM ACCESS MEMORY IN SUBSTITUTION OF A HARD DISK DRIVE	LIN, I-MING
10368945	6947292	150	02/18/2003	PRIMARY FUNCTIONAL CIRCUIT BOARD SUITABLE FOR USE IN VERIFYING CHIP FUNCTION BY ALTERNATIVE MANNER	LIN, I-MING
10392027	6766391	150	03/18/2003	EMBEDDED CONTROL UNIT	LIN, I-MING
10604268	Not Issued	95	07/08/2003	UTILIZING AN ACPI TO MAINTAIN DATA STORED IN A DRAM	LIN, I-MING
10614040	Not Issued	30	07/08/2003	Signal testing of integrated circuit chips	LIN, I-MING
10665294	6963229	150	09/22/2003	CLOCK SKEW INDICATING APPARATUS	LIN, I-MING
10675942	Not Issued	30	10/02/2003	Universal serial bus keyboard control circuitry	LIN, I-MING
10967244	Not Issued	30	10/19/2004	Peel-off nail polish without polish-remover	LIN, I-MING

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** LIN **First Name** I-MING Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

Day : Saturday
Date: 2/18/2006

PALM INTRANET

Time: 21:10:22

Inventor Name Search Result

Your Search was:

Last Name = LIU
First Name = JEN-NAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10614040	Not Issued	30	07/08/2003	Signal testing of integrated circuit chips	LIU, JEN-NAN

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** LIU **First Name** JEN-NAN Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

IEEE Xplore RELEASE 2.1

Search Result - Print Format

< Back t

Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, II CNF = IEE Conference, IEEE STD = IEEE Standard

1. **Test generation for ground bounce in internal logic circuitry**
   Yi-Shing Chang; Gupta, S.K.; Breuer, M.A.;
   VLSI Test Symposium, 1999. Proceedings. 17th IEEE
   25-29 April 1999 Page(s):95 - 104
   IEEE CNF

2. **Ground bounce considerations in DC parametric test generation using boundary scan**
   Majumdar, A.; Komoda, M.; Ayres, T.;
   VLSI Test Symposium, 1998. Proceedings. 16th IEEE
   26-30 April 1998 Page(s):86 - 91
   IEEE CNF

3. **Catch the ground bounce before it hits your system**
   Kurzweil, E.; Lallement, M.; Blanc, R.; Pasquinelli, R.;
   Test Conference, 1993. Proceedings., International
   17-21 Oct. 1993 Page(s):574 - 584
   IEEE CNF

4. **The effect of test system impedance on measurements of ground bounce in printed circuit boards**
   Tzong-Lin Wu; Yen-Hui Lin; Jiuun-Nan Hwang; Jig-Jong Lin;
   Electromagnetic Compatibility, IEEE Transactions on
   Volume 43, Issue 4, Nov. 2001 Page(s):600 - 607
   IEEE JNL

5. **Test generation for maximizing ground bounce for internal circuitry with reconvergent fan-outs**
   Yi-Shing Chang; Gupta, S.; Breuer, M.;
   VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001
   29 April-3 May 2001 Page(s):358 - 366
   IEEE CNF

6. **Ground bounce study of 304 lead interposer MQFP with on-chip decoupling capacitor test die**
   Huang, C.C.; Loh, B.; Wong, F.;
   Northcon 95. I EEE Technical Applications Conference and Workshops Northcon95
   10-12 Oct. 1995 Page(s):343 - 348
   IEEE CNF

7. **Analysis of ground bounce in deep sub-micron circuits**
   Yi-Shing Chang; Gupta, S.K.; Breuer, M.A.;
   VLSI Test Symposium, 1997., 15th IEEE
   27 April-1 May 1997 Page(s):110 - 116
   IEEE CNF

8. **Switching activity generation with automated BIST synthesis for performance testing of interconnects**
   Pendurkar, R.; Chatterjee, A.; Zorian, Y.;
   Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
   Volume 20, Issue 9, Sept. 2001 Page(s):1143 - 1158
   IEEE JNL

9. **A multipath channel model for wideband aeronautical telemetry**
Rice, M.; Davis, A.;
MILCOM 2002. Proceedings
Volume 1, 7-10 Oct. 2002 Page(s):622 - 626 vol.1
IEEE CNF

10. **Embedded robustness IPs**
Dupont, E.; Nicolaidis, M.; Rohr, P.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings
4-8 March 2002 Page(s):244 - 245
IEEE CNF

11. **Elimination of leakage and ground-bounce effects in ground-penetrating radar data**
Abrahamsson, R.; Larsson, E.G.; Li, J.; Habersat, J.; Maksymonko, G.; Bradley, M.;
Statistical Signal Processing, 2001. Proceedings of the 11th IEEE Signal Processing Workshop on
6-8 Aug. 2001 Page(s):150 - 153
IEEE CNF

12. **A noise test structure for CMOS logic families**
Graziano, M.; Masera, G.; Piccinini, G.; Zamboni, M.;
Microelectronics, 1999. ICM '99. The Eleventh International Conference on
22-24 Nov. 1999 Page(s):93 - 96
IEEE CNF

13. **Scaling deeper to submicron: on-line testing to the rescue**
Nicolaidis, M.; Zorian, Y.;
Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings
9-12 March 1999 Page(s):432
IEEE CNF

14. **Synthesis of BIST hardware for performance testing of MCM interconnections**
Pendurkar, R.; Chatterjee, A.; Zorian, Y.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference o
8-12 Nov 1998 Page(s):69 - 73
IEEE CNF

15. **Process aggravated noise (PAN): new validation and test problems**
Breuer, M.A.; Gupta, S.K.;
Test Conference, 1996. Proceedings., International
20-25 Oct. 1996 Page(s):914 - 923
IEEE CNF

16. **Measurement study on simultaneous switching noise**
Chen, L.; Sen, B.;
Electrical Performance of Electronic Packaging, 1995
2-4 Oct. 1995 Page(s):40 - 42
IEEE CNF

17. **Characterization and reduction of simultaneous switching noise for a multilayer package**
Hirano, N.; Miura, M.; Hiruta, Y.; Sudo, T.;
Electronic Components and Technology Conference, 1994. Proceedings., 44th
1-4 May 1994 Page(s):949 - 956
IEEE CNF

18. **Forming damped LRC parasitic circuits in simultaneously switched CMOS output buffers**
Cabara, T.J.; Fischer, W.C.; Harrington, J.; Troutman, W.W.;
Solid-State Circuits, IEEE Journal of

Volume 32, Issue 3, March 1997 Page(s):407 - 418
IEEE JNL

19. **A closed-form solution to the damped RLC circuit with applications to CMOS ground bounce estimation**
Gabara, T.;
ASIC Conference and Exhibit, 1996. Proceedings., Ninth Annual IEEE International
23-27 Sept. 1996 Page(s):73 - 78
IEEE CNF

20. **Modeling the effect of ground bounce on noise margin**
Haydt, M.S.; Owens, R.; Mourad, S.;
Test Conference, 1994. Proceedings., International
2-6 Oct. 1994 Page(s):279 - 285
IEEE CNF

21. **FDTD modeling of the coaxial feed effect on the measurement of the ground bounce in the high speed digit PCB**
Jih-Jong Lin; Tzong-Lin Wu;
Electromagnetic Compatibility, 2000. IEEE International Symposium on
Volume 2, 21-25 Aug. 2000 Page(s):807 - 810 vol.2
IEEE CNF

22. **Design and characterization of an active, EMC-dedicated testchip**
Criel, S.; Bonjean, F.; De Smedt, R.; De Langhe, P.;
Electromagnetic Compatibility, 1999 IEEE International Symposium on
Volume 2, 2-6 Aug. 1999 Page(s):905 - 908 vol.2
IEEE CNF